In the Claims:

Please amend claim 19. The status of the claims is as follows:

1. (Previously Presented) A clock adjustment apparatus for adjusting a phase of a clock signal in a data reproduction system which samples a readout signal from a recording medium in synchronism with the clock signal and reproduces data in accordance with a Viterbi algorithm by using sampled values of the readout signal, said recording medium being recorded with the data modulated in accordance with a recording rule of a predetermined partial response characteristic, said clock adjustment apparatus comprising:

a phase error calculation circuit configured to calculate a phase error of the clock signal based on a difference between first and second sampled values and a difference between second and third sampled values of consecutive first, second and third sampled values of the readout signal; and

an adjusting circuit configured to adjust the phase of the clock signal based on the phase error thereof.

2. (Previously Presented) The clock adjustment apparatus as claimed in claim 1, wherein said phase error calculation circuit calculates the phase error based on a difference between an absolute value of a difference between the first and second sampled values and an absolute value of a difference between the second and third sampled values.

3. (Previously Presented) The clock adjustment apparatus as claimed in claim 1, wherein said phase error calculation circuit continuously calculates the phase error based on all of successive sampled values in an acquisition mode of the clock adjustment apparatus in which pattern data having a highest density is reproduced.

4. (Previously Presented) The clock adjustment apparatus as claimed in claim 1, further comprising:

an edge detection circuit configured to detect an edge portion of the readout signal based on the transition state of the sampled values of the readout signal,

wherein said phase error calculation circuit calculates the phase error of the clock signal based on sampled values of the edge portion of the readout signal detected by said edge detection circuit.

5. (Previously Presented) The clock adjustment apparatus as claimed in claim 4, wherein:

said edge detection circuit comprises a rising edge detection circuit configured to detect a rising edge portion of the readout signal; and

said phase error calculation circuit calculates the phase error of the clock signal based on sampled values of the rising edge portion of the readout signal detected by said rising edge detection circuit.

6. (Previously Presented) The clock adjustment apparatus as claimed in claim 4, wherein:

said edge detection circuit comprises a falling edge detection circuit configured to detect a falling edge portion of the readout signal; and

said phase error calculation circuit calculates the phase error of the clock signal based on sampled values of the falling edge portion of the readout signal detected by said falling edge detection circuit.

7. (Previously Presented) The clock adjustment apparatus as claimed in claim 4, wherein said edge detection circuit detects a portion of the readout signal as the edge portion when the portion comprises a series of successive sampled values in ascending order from a value smaller than a predetermined threshold value to a value larger than the predetermined threshold value, or when the portion comprises a series of successive sampled values in descending order from a value larger than a predetermined threshold value to a value smaller than the predetermined threshold value.

8. (Previously Presented) The clock adjustment apparatus as claimed in claim 7, wherein said edge detection circuit detects the portion of the readout signal as the edge portion when the portion comprises first, second and a third sampled values in an order sampled with the predetermined threshold value being between the first and third sampled

values, and a sign of a difference between the first and second sampled values being identical to that of a difference between the second and third sampled values.

9. (Previously Presented) The clock adjustment apparatus as claimed in claim 7, wherein said edge detection circuit comprises:

an offset estimation circuit configured to estimate an offset of the readout signal caused by an envelope variation thereof; and

a circuit configured to correct the predetermined threshold value in accordance with the offset estimated by said offset estimation circuit.

10. (Previously Presented) The clock adjustment apparatus as claimed in claim 7, further comprising:

a threshold defining circuit configured to define the predetermined threshold value.

11. (Previously Presented) The clock adjustment apparatus as claimed in claim 4, wherein:

said phase error calculation circuit operates in an acquisition mode of the clock adjustment apparatus in which the phase error of the clock signal is continuously calculated based on all of successive sampled values of the readout signal and in a tracking mode of the

clock adjustment apparatus in which the phase error is calculated based on the sampled values of the edge portion of the readout signal detected by said edge detection circuit, and

said clock adjustment apparatus further comprises: an operation mode switching circuit configured to switch an operation mode of said phase error calculation circuit from the acquisition mode to the tracking mode when an amplitude of the phase error calculated by said phase error calculation circuit remains within a predetermined range for a predetermined period of time in the acquisition mode.

12. (Previously Presented) The clock adjustment apparatus as claimed in claim 11, wherein said operation mode switching circuit comprises a convergence time setting circuit which sets the predetermined period of time which is used as a reference when switching the operation mode of the clock adjustment apparatus.

13. (Previously Presented) The clock adjustment apparatus as claimed in claim 11, wherein said operation mode switching circuit comprises a convergence range setting circuit which sets the predetermined range which is used as a reference when switching the operation mode of the clock adjustment apparatus.

14. (Previously Presented) The clock adjustment apparatus as claimed in claim 11, wherein:

said phase error calculation circuit comprises a gain adjustment circuit configured to adjust a gain according to the phase error of the clock signal calculated thereby, so as to adjust the phase of the clock signal using the adjusted gain, and

said clock adjustment apparatus further comprises a gain switching circuit configured to set a first gain with respect to said gain adjustment circuit when said phase error calculation circuit operates in the acquisition mode and to set a second gain, which is smaller than the first gain, with respect to said gain adjustment circuit when said phase error calculation circuit operates in the tracking mode.

15. (Previously Presented) The clock adjustment apparatus as claimed in claim 11, wherein:

said data reproduction system comprises an equalizer which performs a waveform equalization on the sampled values of the readout signal; and

said phase error calculation circuit, in the tracking mode, calculates the phase error of the clock signal based on a transition state of the sampled values on which the waveform equalization has been performed by said equalizer.

16. (Previously Presented) The clock adjustment apparatus as claimed in claim 15, further comprising:

a circuit configured to prevent the phase error calculated by said phase error calculation circuit from being used to adjust the phase of the clock signal during a predetermined period of time before and after the sampled values to be used by said phase error calculation circuit to calculate the phase error switch to the sampled values subjected to the waveform equalization by said equalizer.

17. (Previously Presented) The clock adjustment apparatus as claimed in claim 1, further comprising:

a normalization circuit configured to normalize the phase error of the clock signal calculated by said phase error calculation circuit so that a transfer function of a feedback loop for adjusting the phase of the clock signal remains constant.

18. (Previously Presented) A clock adjustment apparatus for adjusting a phase of a clock signal in a data reproduction system which samples a readout signal from a recording medium in synchronism with the clock signal, and reproduces data in accordance with a Viterbi algorithm by using sampled values of the readout signal, said recording medium being recorded with the data modulated in accordance with a recording rule of a predetermined partial response characteristic, said clock adjustment apparatus comprising:

a phase error calculation circuit configured to calculate a phase error of the clock signal based on a transition state of the sampled values of the readout signal before undergoing the Viterbi algorithm; and

an adjusting circuit configured to adjust the phase of the clock signal based on the phase error thereof.

19. (Currently Amended) An apparatus comprising:

a data reproduction system configured to sample a readout signal from a recording medium in synchronism with a clock signal, and to reproduce data in accordance with a Viterbi algorithm by using sampled values of the readout signal, said recording medium being recorded with the data modulated in accordance with a recording rule of a predetermined partial response characteristic,

said data reproduction system comprising a clock adjustment circuit configured to calculate a phase error of the clock signal based on ~~the~~ a difference between first and second sampled values and a difference between second and third sampled values of consecutive first, second and third sampled values of the readout signal, and to adjust a phase of the clock signal based on the phase error.

20. (Previously Presented) The apparatus as claimed in claim 19, wherein the recording medium comprises an optical disk.